Jingyan JOURDAN-LU

Post-doc at Inria

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Summary

Current research interest:

Equivalence checking for asynchronous concurrent systems.

Experience on floating-point airthmetic:

1. Compiler optimization development for Floating-Point (FP) support.
2. Algorithms and implementations for FP arithmetic.
3. Benchmarking and performance analysis of FP applications.

Experience on embedded systems:

1. Signal processing and Zigbee network applications on MCUs and DSPs.
2. Drivers, BSPs for WinCE, Microsoft .Net Micro Framework.

Specialties: Verification, Compiler development, FP arithmetic, Numerical algorithms, Digital signal processing, Embedded software, Microprocessors, Computer architecture

Experience

Post-doc in Convecs team at Inria

2012 - Present (1 year)

Equivalence checking for asynchronous concurrent systems.

Software engineer in Compilation Expertise Center at STMicroelectronics

2009 - 2012 (3 years)

Advanced compilation optimizations for FP applications, focusing on development in the C/C++ Open64 compiler for the selection of FP operators and range analysis.

PhD student in Aric team at ENS Lyon

2009 - 2012 (3 years)

Algorithms and implementations for Floating-Point arithmetic (IEEE754 standard) on integer-only processors, focusing on FMA, non-generic operators (such as dot products and scaling operators) and trigonometric functions.

System engineer at Atmel Corporation

2007 - 2007 (less than a year)

Development of the BSP supporting ATMEL ARM based chips for Microsoft .Net Micro Framework.

Software engineer (internship) at Atmel Corporation
2004 - 2007 (3 years)

DSP project. Development of demo applications, libraries, drivers and hardware testing programs for a dual-core DSP.

Zigbee Transceiver. Development of Zigbee sniffer, PC-side debugger and a demo application based on WinCE BSP of AT91SAM9261.

Education

École Normale Supérieure de Lyon (ENS-Lyon)
Doctor, Computer Science, 2009 - 2012

East China Normal University (ECNU)
Bachelor/Master, Electronic Engineering, 2000 - 2007

Skills & Expertise

Algorithms
Compilation
Numerical Analysis
Numerical Software
Embedded Systems
Microprocessors
Chinese
English
French

Publications

Simultaneous floating-point sine and cosine for VLIW integer processors
23rd IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP) 2012

Authors: Jingyan JOURDAN-LU, Claude-Pierre JEANNEROD

Graphics and signal processing applications often require that sines and cosines be evaluated at a same floating-point argument, and in such cases a very fast computation of the pair of values is desirable. This paper studies how 32-bit VLIW integer architectures can be exploited in order to perform this task accurately for IEEE single precision. We describe software implementations for sinf, cosf, and sincosf over [-pi/4,pi/4] that have a proven 1-ulp accuracy and whose latency on STMicroelectronics' ST231 VLIW integer processor is 19, 18, and 19 cycles, respectively. Such performances are obtained by introducing a novel algorithm for simultaneous sine and cosine that combines univariate and bivariate polynomial evaluation schemes.

Non-generic floating-point software support for embedded media processing
7th IEEE International Symposium on Industrial Embedded Systems (SIES) 2012

Authors: Jingyan JOURDAN-LU, ClaudePierre Jeannerod, Christophe Monat

This paper presents some work in progress on the design and implementation of efficient floating-point software support for embedded integer processors. We provide quantitative evidence of the benefits of supporting various non-generic (that is, specialized, fused, or paired) operations in addition to the five basic arithmetic operations: for individual calls, speedups range from 1.12 to 4.86, while on DSP kernels and benchmarks, our approach allows us to be up to 1.34x faster.

How to square floats accurately and efficiently on the ST231 integer processor
20th IEEE Symposium on Computer Arithmetic (ARITH) July 25, 2011
Authors: Jingyan JOURDAN-LU, Claude-Pierre JEANNEROD, Christophe MONAT, Guillaume REVY

We consider the problem of computing IEEE floating-point squares by means of integer arithmetic. We show how the specific properties of squaring can be exploited in order to design and implement algorithms that have much lower latency than those for general multiplication, while still guaranteeing correct rounding. Our algorithm descriptions are parameterized by the floating-point format, aim at high instruction-level parallelism (ILP) exposure, and cover all rounding modes. We show further that their C implementation for the binary32 format yields efficient codes for targets like the ST231 VLIW integer processor from STMicroelectronics, with a latency at least 1.75x smaller than that of general multiplication in the same context.

Techniques and tools for implementing IEEE 754 floating-point arithmetic on VLIW integer processors
International Workshop on Parallel and Symbolic Computation (PASCO) July 21, 2010
Authors: Jingyan JOURDAN-LU, Christian BERTIN, Claude-Pierre JEANNEROD, Hervé KNOCHEL, Christophe MONAT, Christophe MOUILLERON, Jean-Michel MULLER, Guillaume REVY

Recently, some high-performance IEEE 754 single precision floating-point software has been designed, which aims at best exploiting some features (integer arithmetic, parallelism) of the STMicroelectronics ST200 Very Long Instruction Word (VLIW) processor. We review here the techniques and software tools used or developed for this design and its implementation, and how they allowed very high instruction-level parallelism (ILP) exposure. Those key points include a hierarchical description of function evaluation algorithms, the exploitation of the standard encoding of floating-point data, the automatic generation of fast and accurate polynomial evaluation schemes, and some compiler optimizations.

NLMS-Based AEDA Algorithm for Sound Source Localization
Journal of East China Normal University, Natural Sc, 2007(5): 113-117 2007
Authors: Jingyan JOURDAN-LU, Shouzheng ZHU

To speed conventional Adaptive Eigenvalue Decomposition Algorithm (AEDA), an NLMS-based optimized AEDA algorithm was proposed. It gives better performance for convergence, which makes it possible for real-time applications. Experimental results showed that this method can work well in sound source localization.
