Job offer: Software engineer (m/f) – Formal methods and verification of hardware circuits

Type of position: R&D engineer
Place of work: Inria research center, Montbonnot St Martin (France)
Research topics: Formal methods and verification of circuits
Research team: CONVECS (http://convecs.inria.fr)
Contract duration: 12 month (extension possible)
Starting date: December 1st, 2017
Salary: from 30700 euros gross, according to diplomas and experience
Application deadline: October 31, 2017
Submit application on-line at https://jobs.inria.fr/public/classic/en/offres/2017-00011
Contact for information about the position: Hubert Garavel (hubert.garavel@inria.fr)

About Inria and the job

Inria, the French National Institute for computer science and applied mathematics, promotes “scientific excellence for technology transfer and society”. Graduates from the world’s top universities, Inria's 2,700 employees rise to the challenges of digital sciences. With its open, agile model, Inria is able to explore original approaches with its partners in industry and academia and provide an efficient response to the multidisciplinary and application challenges of the digital transformation. Inria is the source of many innovations that add value and create jobs.

The Inria research center of Grenoble - Rhône Alpes gathers nearly 730 workers organized in 34 research teams and 9 services that support research.

The proposed job takes place within the CONVECS team, which is shared between Inria, CNRS, Grenoble INP and University Grenoble Alpes.

Mission

The proposed job is part of the French research project Securiot-2 that aims at developing novel methods to enable the design and certification of circuits for the Internet of Things. The goal is to improve the CADP verification toolbox (http://cadp.inria.fr) developed by the CONVECS team and to apply this toolbox to verify whether a circuit is robust with respect to faults.

Job offer description

The planned activities will consist, on the one hand, in participating to the formal description of the examples of circuits under scrutiny, in modelling various faults (either transient or permanent) at the logical-gate level, and to study the impact of such faults on the circuit behaviour, and, on the other hand, in contributing to enhancements of the CADP software tools according to the needs that will arise during the project.

Skills and profile

Diplomas : engineering degree, master degree, or PhD in computer science. The expected skills are proficiency in software programming and intellectual rigour in verification and testing activities. Knowledge about formal methods, and/or skills in C-language programming, and/or competences in hardware circuit design would be an asset.

Benefits

- Restaurant on site
- Financial participation for public transport
- Social and sporting activities
- French courses

Additional Information

Security and defense procedure: This position might be situated in a restricted area (ZRR), as defined in Decree No. 2011-1425 relating to the protection of national scientific and technical potential (PPST). Authorisation to enter an area is granted by the director of the unit, following a favourable Ministerial decision, as defined in the decree of July 3, 2012 relating to the PPST. An unfavourable Ministerial decision in respect of a position situated in a ZRR would result in the cancellation of the appointment.