Formal Analysis of the ACE specification for Cache Coherent Systems-on-Chip (SoC)

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System-Level Cache Coherency for Heterogeneous SoCs

Components without caches:
- Accelerators
- I/O Blocks
- Dedicated IPs
- Interconnects

Components with caches:
- Processors (with caches)
- Memory

Formally Modeling an ACE-compliant SoC using CADP (http://cadp.inria.fr)

- Modular toolbox for asynchronous systems: formal modeling & verification, simulation
- Based on concurrency theory
- User-friendly input language

Model overview

Verified Properties in MCL (Model Checking Language)

Complete Execution of Transactions

```
```

Cache Coherency

```
true +

{ 0 false . Tim.X Bin . Tim.M Bin "ACE_UD" .
   (not (false . Tim.X Bin . Tim.M Bin "ACE_UD") ) } +

{ 0 false . Tim.M Bin . Tim.X Bin . String . where s1="ACE_UD") } +

false
```

Data Integrity

```
true +

{ 0 "WRITEBACK" ?n: Bin . ?l: Not . ?m: Bin }

( not (false . "WRITEBACK" ) +

{ 0 "WRITEBACK" } +

( not (true . "ACE_UD") ) .

{ 0 "ACE_UD" . "WRITEBACK" . "ACE_UD" } .

{ true . "ACE_UD" . } .

{ 0 "WRITEBACK" . "ACE_UD" } +

( not (true . "ACE_UD") ) .

{ 0 "ACE_UD" . } .

false
```

Perspectives

- Generic interconnect model for analyzing impact of a coherent interconnect in a model of a concrete SoC
- Model-based test and validation: automatic test-scenario extraction and guided (co-)simulation

References